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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,553	YANCE ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson et al., U.S. Patent No. 5,315,161 in view of Kikuchi et al., U.S. Patent No. 6,038,515.

Regarding claim 1, Robinson discloses a method for controlling a microcomputer in a microcomputer system (Abstract, lines 1-5, FIG. 1), the microcomputer system including a backup power supply for supplying the clock with power for a predetermined time (column 2, lines 40-42, lines 65-68, column 3, lines 1-5, lines 43-46), said method comprising:

determining whether power is recovered within a given time period (column 3, lines 5-7, column 5, lines 53-55); and

switching to the high speed operation mode in response to determining that the power is recovered within the given time period,

[Robinson does not specifically state switching to the high speed operation mode in response to determining that the power is recovered within the given period. However, Robinson discloses not executing the shut down procedure if the primary power (i.e. AC power) is restored during the ride-through period (column 3, lines 5-7, column 5, lines 53-55) and returning the computer to normal running state (column 5, lines 39 and 40, FIG. 3, S2). During "normal running state" the computer requires higher performance (i.e. execution with higher speed clock frequency) in comparison to low speed mode when the clock is reduced. Thus, the normal running state disclosed by Robinson would necessarily be a high speed operation mode.]

wherein the clock measures the given time period in the low speed mode.

[Robinson does not specifically state wherein the clock measures the given time period in the low speed mode. However, Robinson discloses an orderly system shutdown during which a shut down counter is decremented (column 5, lines 58-60). In addition, Robinson discloses system operation for a short period after the orderly shutdown has completed prior of turning the power off (column 6, lines 22-28). Thus, Robinson discloses system operation (i.e. presence of system clock) during system shutdown (with duration controlled by the shut down counter clocked by the clock) and for a short period after shutdown completion. Therefore, during and after orderly shutdown (i.e. the system entering or has entered low speed mode) the clock is still running, and thus Robinson discloses the clock measures the given time period in the low speed mode.]

Robinson fails to disclose detecting a disconnection of the microcomputer system from a power supply and switching from the high speed operation mode to the low speed operation mode in response to detecting the disconnection.

Kikuchi teaches a portable information terminal apparatus, which can correctly detect a power supply voltage (column 1, lines 8-10). In addition, Kikuchi teaches determining whether the power supply is turned OFF (i.e. detecting whether the system is electrically disconnected from a power supply) and in that case, switching the information terminal apparatus to an operational state having the smallest power consumption quantity (column 7, lines 55-63, FIG. 6 SA14, SA15). Thus, Kikuchi teaches detecting an electrical disconnection of the system from the power supply, in response to which switching to the smallest power consumption mode. In Kikuchi, the above-mentioned method for detecting power supply voltage is used to prevent erroneous operation due to decrease of a power supply voltage (column 2, lines 28-30). Thus, the stored data and programs can be prevented from being destroyed because of the erroneous operation (column 2, lines 31-34), and thus reliability is ensured.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above-described method for detecting a disconnection of the system from a power supply and switching to the smallest power consumption mode in response to that detection, as suggested by Kikuchi with the method disclosed by Robinson in order to implement detecting a disconnection of the microcomputer system from a power supply and switching from the high speed operation mode to the low speed operation mode in response to detecting the disconnection. One of ordinary

skill in the art would be motivated to do so in order to ensure reliable operation in the microcomputer system.

Regarding claim 3, Robinson further discloses the method, further comprising setting the microcomputer to a stop operation mode unless the power is recovered within the given time period (Abstract, lines 5-8).

Re claim 4, Robinson further discloses the method, further comprising storing a value representing a time period, which the microcomputer measures during power shutdown addressed previously.

[Robinson does not specifically state storing a value representing a time period in a volatile memory of the microcomputer system. The examiner takes Official Notice that storing a value representing a time period in volatile memory is common in the art. It is well known in the art that timers storing a value representing a time period are implemented with registers, which are a type of volatile memory. Using volatile memory allows flexibility when a user sets the timers for example. Robinson discloses user settable timer values controlling the shutdown process (column 2, lines 3-5, column 7, lines 37-39). Accordingly, it would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to store a value representing a time period in a volatile memory of the microcomputer system. One of ordinary skill in the art would be motivated to do so in order to achieve flexibility for the user settable timer values used during the shutdown process.]

Claims 5, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson et al., U.S. Patent No. 5,315,161 in view of Kikuchi et al., U.S. Patent No. 6,038,515, and further in view of Bilir, U.S. Patent No. 5,923,099.

Regarding claim 5, Robinson and Kikuchi disclose all claim limitations as per claim 1. In addition, Robinson discloses periodically determining whether power is recovered within a first given time period (column 5, lines 43-55, column 6, lines 54-63) and a second given time period which is longer than the first given time period.

[Robinson does not specifically state a second given time period which is longer than the first given time period. However, Robinson discloses a shutdown procedure controlled by a shutdown timer (i.e. second given time period) (column 5, lines 58-60), the procedure initiated after the completion of the ride-through period (first given period) (column 6, lines 64-67, column 7, lines 1-7). Robinson further discloses that the duration for both the ride-through and the shutdown time periods are user settable (column 2, lines 3-5, column 7, lines 37-39) with the user having the possibility to minimize the ride-through time period (first given period) and maximize the shut down time period (second given time period) (column 7, lines 45-48). Thus, Robinson discloses a second given time period which is longer than the first given time period.]

Robinson and Kikuchi fail to disclose setting the microcomputer to a stop operation to stop operation of the microcomputer unless the power is recovered within a second given time period.

Bilir teaches an intelligent backup controller performing graceful shutdown of processing system upon loss of main AC power (Abstract, lines 1-3). Bilir further teaches triggering a first timer beginning with detection of the switch from main AC power to backup power, triggering a second timer (second given time period) upon receipt of a shutdown complete indication from the operating system, and terminating provision at the expiration of either timer unless main AC power is restored during the

process (Abstract, lines 8-13). Thus, the processing system is powered off (operation stopped) (column 3, lines 38-41) unless the AC power is recovered during the time period controlled by the second timer (column 4, lines 32-34). In Bilir, upon detection of external AC power, the system graceful shutdown sequence is interrupted and the shutdown process is aborted (column 3, lines 49-53). Thus, the system is sensitive to the current operation status and the system graceful shutdown is only implemented after ascertaining that it is safe to do so automatically in a non-disruptive manner (column 1, lines 37-41).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the graceful shutdown (powering off) method for a processing system unless the external AC power is restored during a second period, as suggested by Bilir for the method disclosed by Robinson and Kikuchi in order to implement setting the microcomputer to a stop operation to stop operation of the microcomputer unless the power is recovered within a second given time period. One of ordinary skill in the art would be motivated to do so in order to ensure safe (non-disruptive) automatic microcomputer shutdown.

Regarding claim 6, Robinson, Kikuchi, and Bilir disclose the method as per claim 5, but does not specifically state the second given time period is set to be longer than the first given time period by substantially an integral of the first given time period. However, Robinson does not impose any restrictions on the user selectable time value for the second given period (column 2, lines 3-5, column 7, lines 37-39). Thus, Robinson discloses the second given time period is set to be longer than the first given time period by substantially an integral of the first given time period.

Regarding claim 7, Robinson further discloses the method, further comprising storing a value representing a time period, which the microcomputer measures during power shutdown addressed previously.

[Robinson does not specifically state storing a value representing a time period in a volatile memory of the microcomputer system. The examiner takes Official Notice that storing a value representing a time period in volatile memory is common in the art. It is well known in the art that timers storing a value representing a time period are implemented with registers, which are a type of volatile memory. Using volatile memory allows flexibility when a user sets the timers for example. Robinson discloses user settable timer values controlling the shutdown process (column 2, lines 3-5, column 7, lines 37-39). Accordingly, it would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to store a value representing a time period in a volatile memory of the microcomputer system. One of ordinary skill in the art would be motivated to do so in order to achieve flexibility for the user settable timer values used during the shutdown process.]

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson et al., U.S. Patent No. 5,315,161 in view of Kikuchi et al., U.S. Patent No. 6,038,515, further in view of Bilir, U.S. Patent No. 5,923,099, and further in view of Fukazawa, Japanese Pat. No. JP 06067749.

Regarding claim 8, Robinson, Kikuchi, and Bilir disclose all claim limitations as per claim 5.

Robinson, Kikuchi, and Bilir fail to disclose checking whether the clock is set, setting the microcomputer to a stop operation mode to stop an operation of the

microcomputer unless the clock is set, and switching from the high speed operation mode to the low speed operation mode when the clock is set.

Fukazawa teaches high speed operation in an electric apparatus where a clock is set (Abstract, lines 5-9). Fukazawa further teaches in case of power interruption during the high speed operation switching to a slow mode or stop mode based on whether the clock was set or not (Abstract, lines 9-14). In addition, Fukazawa teaches slow speed operation in the slow mode and stopping the clock in stop mode (Abstract, lines 14-16). Fukazawa does not specifically state checking whether the clock is set. However, in order to proceed with switching to either the slow or stop mode based on the clock being set or not, Fukazawa inherently teaches checking whether the clock is set. In Fukazawa, the above-mentioned method decreases the power consumption and prolongs the backup battery life.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the method of switching to from high speed operation to either a slow mode or a stop mode bases on whether a clock was set, as suggested by Fukazawa for the method disclosed by Robinson, Kikuchi, and Bilir in order to implement checking whether the clock is set, setting the microcomputer to a stop operation mode to stop an operation of the microcomputer unless the clock is set, and switching from the high speed operation mode to the low speed operation mode when the clock is set. One of ordinary skill in the art would be motivated to do so in order to decrease the power consumption and prolong the backup battery life.

Regarding claim 9, Robinson further discloses the method, further comprising storing a value representing a time period, which the microcomputer measures during power shutdown addressed previously.

[Robinson does not specifically state storing a value representing a time period in a volatile memory of the microcomputer system. The examiner takes Official Notice that storing a value representing a time period in volatile memory is common in the art. It is well known in the art that timers storing a value representing a time period are implemented with registers, which are a type of volatile memory. Using volatile memory allows flexibility when a user sets the timers for example. Robinson discloses user settable timer values controlling the shutdown process (column 2, lines 3-5, column 7, lines 37-39). Accordingly, it would have been obvious to one of the ordinary skill in the art at the time of the applicant's invention to store a value representing a time period in a volatile memory of the microcomputer system. One of ordinary skill in the art would be motivated to do so in order to achieve flexibility for the user settable timer values used during the shutdown process.]

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

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SUPERVISORY PATENT EXAMINER
11/29/06